

10/31/00

JC954 U.S. PTO

11-01-00

**PATENT APPLICATION TRANSMITTAL LETTER**  
(Large Entity)Docket No.  
INTL-0438-US (P9450)TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

**BENJAMIN M. CAHILL, III**For: **ANALYZING ALPHA VALUES FOR FLICKER FILTERING**

Enclosed are:

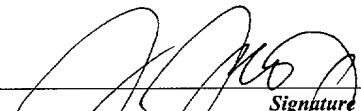
- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL669041522US**
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<b>Total Claims</b>	22	- 20 =	2	x \$18.00	\$36.00
<b>Indep. Claims</b>	3	- 3 =	0	x \$80.00	\$0.00
<b>Multiple Dependent Claims (check if applicable)</b> <input type="checkbox"/>					\$0.00
<b>BASIC FEE</b>					\$710.00
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**APPLICATION**

**FOR**

**UNITED STATES PATENT**

**TITLE:** **ANALYZING ALPHA VALUES FOR FLICKER  
FILTERING**

**INVENTOR:** **BENJAMIN M. CAHILL, III**

Express Mail No.: EL669041522US

Date: October 31, 2000

## ANALYZING ALPHA VALUES FOR FLICKER FILTERING

### Background

This invention relates to mixing graphics and video and, more particularly, to selective use of flicker filtering operations.

5 Motion video signals such as television programming may be combined with static signals generated by a processor-based system. The static signals are known as personal computer (PC) graphics signals, or simply graphics signals. The combined signal may be viewed on a television monitor.

10 A set-top box is a processor-based system that employs a television display instead of a computer monitor for viewing video signals, PC graphics signals, or a combination of the two. The set-top box may execute application software, such as electronic mail programs, connect to a data network, such as the Internet using browser software, and receive and display television programming signals.

15 Set-top boxes may combine a broadcast video signal with a graphics signal. The set-top box receives the video signal from an external source, such as via a coaxial cable, and mixes the signal with the PC graphics signal, typically generated from within the set-top box.

20 The set-top box may employ alpha values when combining the video signal with the PC graphic signal. Where a pixel, or picture element, results from the combination of a video element and a PC graphics element, an alpha value describes the weight of the elements, usually expressed as a percentage. The resulting pixel may be solid graphics, transparent graphics with video, solid video, and so on. The combining operation is known as alpha blending.

25 The television display receives video signals as a series of alternating fields: an odd field consisting of odd lines followed by an even field consisting of

even lines, for example. The signal received by the television display is known as interlaced video. One odd field plus one even field constitutes a frame of the video signal.

One phenomenon of interlaced transmission is flickering. Flickering occurs when the video image includes small graphic detail, such as a single horizontal line, or other fine detail. For example, in an image including the letter "A", the horizontal line in the letter may flicker as every other field is being displayed. Where the small detail (the horizontal line) appears in only one field, the line comes, then goes, as alternating odd and even fields are displayed.

Flicker filtering enhances graphics displayed on an interlaced monitor, such as a household television set. Flicker filtering blends pixels from scan lines of a field with adjacent scan lines from an associated, or opposite polarity, field. Thus, for example, where small graphic detail occupies a single scan line in an odd field, scan lines that would be displayed adjacent to the scan line in an even field may be updated to also include a weighted portion of the small graphic detail. By blending adjacent scan lines, the small detail image remains visible on the display, and flickering is lessened.

Flicker filtering may adversely affect motion video images, however. While the flicker filter generally may improve the appearance of the static graphics image, flicker filtering may also blur the detail of the video image. Further, flicker filtering allows images from two different instances of time (e.g., odd field, and even field) to "appear" on the display simultaneously. This tends to blur the image in time, particularly for moderately fast horizontal pans and action-laden scenes. Thus, although flicker filtering is beneficial for graphics images, it may diminish image quality for video images.

Thus, there is a continuing need to analyze the alpha blending value before performing flicker filtering operations.

### Brief Description of the Drawings

Figure 1 is a block diagram of a system according to one embodiment of the invention;

5 Figure 2 is a diagram of a display illustrating a fine graphics image according to one embodiment of the invention;

Figures 3A and 3B are diagrams illustrating the display when alternate fields are visible according to one embodiment of the invention;

Figure 4 is a diagram of the fine graphic image following a flicker filtering operation according to one embodiment of the invention;

10 Figure 5 is a table associating alpha values with flicker filter levels according to one embodiment of the invention;

Figure 6 is a flow diagram showing operation of the system according to one embodiment of the invention; and

15 Figure 7 is a table associating the alpha values with the flicker filter levels following the software operations of Figure 6 according to one embodiment of the invention.

### Detailed Description

20 In accordance with the embodiments described herein, a flicker filter is adjusted when certain alpha blending operations occur. The operations specify the strength of a graphics signal to be displayed simultaneously with a video signal. For some weakly showing graphics signals, the flicker filter may be turned off entirely.

25 In Figure 1, a system 100 includes a processor 10 connected to a system bus 12, according to one embodiment. The system 100 may be any of a variety of processor-based systems, including a personal computer, an Internet appliance, a set-top box, and so on.

A multi-function bridge 22 is connected to the system bus 12. The bridge 22 may itself include memory control functions. In one embodiment, the bridge 22 interfaces to a system memory 40 as well as a flash/ROM 18.

5 The memory 40 may be a random access memory (RAM) such as dynamic random access memory (DRAM), synchronous DRAM (SDRAM), static RAM (SRAM), a Rambus® DRAM (RDRAM), or other suitable volatile media. The flash/read-only memory (ROM) 18 may store one or more software programs 80, for execution by the processor 10.

10 In one embodiment, the bridge 22 is further connected to a peripheral component interconnect (PCI) bus 24. The PCI Specification is available from The PCI Special Interest Group, Portland, Oregon 97214. The PCI bus is a high-performance bus for connecting I/O processors, buses, controllers, and the like.

15 The system 100 further includes a graphics controller 14, coupled to the PCI bus 24. In one embodiment, a Tvia CyberPro™ 5000 streaming media processor, suitable for set-top boxes and Internet appliances, available from Tvia Technologies, Inc., Santa Clara, California, is operable as the graphics controller 14.

20 The graphics controller 14 may include circuitry for performing a variety of video operations. The graphics controller 14 may include graphics engines, for rendering graphics images, an alpha blender, a video mixer, a video scaler, a color burst generator, a pixel clock, an analog television encoder, and a flicker filter, to name but a few possible components. Furthermore, the elements may be combined, such as where the television encoder also includes a color burst generator. The described features are illustrative only.

25 A video signal 38 may be received into the system 100 through a cable or other connector IN 30. In one embodiment, the video signal 38 is received into a tuner/capture device 28, which converts radio frequency (RF) signals into baseband composite video, for receipt by a video decoder 26. The video

decoder 26 decodes the baseband video signal and digitizes the signal into luma and chroma components. The components may then be received into the graphics controller 14 using a dedicated video port. The graphics controller 14 may send the components into a graphics memory 16, also known as a frame buffer memory 16. Alternatively, the graphics controller 14 may bypass the frame buffer memory 16, such as for performing real-time processing operations.

In one embodiment, the system 100 further includes a stereo decoder 36. The stereo decoder 36 receives the baseband composite video signal from the tuner/capture card 28, and decodes baseband sound signals into stereo, for receipt by an audio encoder/decoder (codec) 32. The audio codec 32 may connect to a speaker 34 that, in one embodiment, is external to the system 100.

In one embodiment, the graphics controller 14 produces graphics signals. The internally generated graphics signal may be mixed with the incoming video signal, such as in a video mixer or an overlay, for example (not shown). Whether mixed or not, an outgoing, or display signal 42 is received by a television monitor 20, which is external to the system 100 according to one embodiment.

Thus, the display signal 42 may be a video signal received into the system 100 by the cable IN 30, a graphics signal generated inside the system 100, a combination of the video and graphics signals, a combination of multiple video signals, and so on. The term "display signal" is used throughout this document to identify any possible signal that is made suitable for receipt by the television monitor 20.

Increasingly, analog video signals from an external source are combined with graphics signals typically created within the set-top box, or other processor-based system, before being displayed. For example, a graphics image may be superimposed on a video image such that both are visible simultaneously. Some television networks, for example, display an identification icon in the lower right-

hand corner of the television display while a program is broadcast. The graphics icon is typically transparent enough that the video image is not disturbed. Graphics images may include fine detail, such as with text, or may be coarse, such as with a blue background co-incident with scrolling stock quotes.

5           As explained in the background, television displays expect incoming signals to be interlaced. That is, an odd field of the video signal 42 is received, followed by an even field, and so on. The television display raster includes hundreds of scan lines. When the odd field is received, the television monitor 20 displays the odd scan lines; when the even field is received, the television  
10       monitor 20 receives the even scan lines.

          The television monitor 20 receives these odd and even fields several times each second. For example, according to the Television Standard of the National Television Systems Committee (NTSC), an interlaced color composite signal includes 525 scan lines, is interlaced 2:1, and has a 59.95 Hz field rate (NTSC,  
15       1953). According to the Phase Alternation by Line (PAL) standard, an interlaced color composite signal has 625 scan lines and a 50 Hz field rate (PAL, 1967).

          Particularly for still images, interlaced display of graphics signals may cause a noticeable flicker of the image. A flicker results when part of the image occupies a single scan line, such as an image having thin, horizontal lines. In  
20       Figure 2, for example, a text letter "A" occupies a number of scan lines 52 of a display 50. The scan lines 52 include odd scan lines 52o and even scan lines 52e.

          The letter "A" includes two diagonal lines, meeting at the top, and a horizontal line 60 connecting approximately in the middle, between the two  
25       diagonal lines. The horizontal line 60 that forms a part of the "A" occupies a single scan line 54.

          In Figure 3A, the odd scan lines 52o of the "A" are sent to the display 50. In this image, the horizontal line 60 of the "A," in scan line 54, is visible. In



Figure 3B, however, only the even scan lines 52e of the display 50 receive signal information. Now, the horizontal line 60 is not visible. Accordingly, displaying the image of Figure 3A, followed rapidly by the image of Figure 3B, produces flicker. (The diagonal components of the "A" likewise may produce flicker, but tend to be less noticeable than the horizontal line 60.)

To address this phenomenon, a flicker filtering operation may be performed on the signal to be displayed, typically from within the graphics controller 14. Flicker filtering blends pixels from scan lines of a given field with adjacent scan lines from one or more opposite fields. The blending reduces flicker caused by small graphics detail, such as the single horizontal line 60. Where originally the small detail appears in only one field, the flicker filtering makes the detail "appear" in both fields.

In Figure 4, the "A" is shown, this time following flicker filtering. A scan line 58 includes a gray horizontal line 56. Likewise, a scan line 64 includes a gray horizontal line 62. Both horizontal lines 56 and 62 are adjacent to the horizontal line 60 in scan line 54, line 56 on one side and line 62 on the other side. The scan line 58 and the scan line 64 include both diagonal components of the "A" and a gray representation of the horizontal line 60 from the adjacent scan line 54. The information that produces the flicker (the horizontal bar 60) is thus also present on the adjacent scan lines 58 and 64.

One method of flicker filtering is to employ a filter such as a finite impulse response (FIR) filter. Some flicker filters include the ability to adjust the FIR filter, for example, by increasing the number of taps, or by adjusting the weight of each tap. The FIR flicker filter thus may include multiple levels or strengths.

While flicker filtering may mitigate the flickering effects of interlaced graphics, flicker filtering also may disturb motion video such as a movie or television program. After flicker filtering, the static video detail of a movie may be blurred. Further, because flicker filter uses information from an adjacent

field, images from two different instances in time may “appear” on the display simultaneously, blurring the image in time. Such is particularly evident in moderately fast horizontal pans or in action-oriented scenes.

5 In some prior art systems, flicker filtering is performed for all types of display signals, whether graphics, video, or mixed video and graphics signals. For other systems, an option may permit flicker filtering to be turned on or off, as desired.

10 According to one embodiment, flicker filtering is adjusted according to the “strength” of the graphics image being displayed. In other words, an assessment of the degree of alpha blending is made. The strength of the graphics image may be identified by the alpha value. A weakly showing, or more transparent, graphics image typically will not generate enough contrast in the combined image to induce a perception of flicker. Because flicker filtering may disturb the underlying video image, where a somewhat transparent graphics  
15 image is being displayed, the flicker filter is turned off.

In one embodiment, an eight-bit alpha value specifies the strength of a graphics image to be displayed simultaneously with a video image, for a total of two hundred and fifty-six possible “strengths.” A flicker filter likewise may include eight levels of flicker filtering, according to one embodiment.

20 In Figure 5, a table relates alpha values to the flicker filter levels, according to one embodiment. Alpha values from 0-32 result in flicker filter level 0, or no flicker filter, alpha values 33-40 result in flicker filter level 1, and so on. Alpha values 91-255 invoke the highest flicker filter level, level 7, according to one embodiment. In the mid-range, the flicker filter level increases for every  
25 eight increments of the alpha value. The “alpha step size” is thus eight for this flicker filter. An alpha value of 33 represents a threshold, below which no flicker filtering is performed.

Because some transparent graphic images do not induce enough flicker to justify flicker filtering, in one embodiment, the system 100 monitors the alpha value and adjusts the flicker filter level, as needed, for low alpha values. The monitoring and adjusting may, for example, be performed by the software 80 of Figure 1. The operation of monitoring and adjusting, according to one embodiment, is depicted in the flow diagram of Figure 6.

The alpha value associated with the current image being sent to the display is compared to a predefined threshold value (diamond 82). In one embodiment, this threshold value is empirically determined to be the alpha value below which no flicker filtering is to be performed. In other words, the threshold identifies graphics images of sufficiently low strength that no flicker is noticeable in the absence of flicker filtering. Accordingly, by not flicker filtering, the possible adverse affects to the video image may be avoided.

In a second embodiment, the threshold value is not predetermined, but is based upon an evaluation of the image prior to being displayed. In other words, the threshold value may be generated by the software 80 based upon certain image qualities.

Where the alpha value does not exceed the predetermined threshold value (the "no" prong of diamond 82), in one embodiment, the flicker filter is turned off, or set to level "0" (block 84), and no flicker filtering is performed. Where the alpha value exceeds the predetermined threshold value (or is identical to same), however, the flicker filter may nevertheless be adjusted. For example, in one embodiment, a calculation for a new flicker filter level is performed (block 86).

Once a new filter level is calculated, the level is compared to a value corresponding to the highest flicker filter level (diamond 88). If the calculated filter level exceeds the highest level of the flicker filter, the filter level is simply

set to the highest level of the flicker filter (block 90). Otherwise, the flicker filter level is adjusted according to the calculation (block 92).

In Figure 6, the predetermined threshold value is subtracted from the current alpha value. The result is divided by the alpha step size for a whole number result. A constant value of 1 is added to the whole number result. The formula is one of many possible calculations that may be performed, which relates the filter level to the alpha value. Alternatively, a lookup table may be employed which associates alpha values with the new filter levels.

A table associating the alpha values with the adjusted flicker filter levels, based upon the formula used in Figure 6, is depicted in Figure 7, where the alpha step size is 8 and the predetermined threshold value is 81. The eight available flicker filter levels are still invoked, but for higher alpha values, as shown.

Thus, according to the embodiments described herein, a flicker filter is adjusted based upon the strength of the graphics image to be displayed simultaneously with a video image. In one embodiment, a comparison between the alpha values and a predetermined threshold value is used to calculate the new flicker filter levels. For sufficiently low alpha values corresponding to transparent graphics images, the flicker filter is turned off entirely, in some embodiments. Accordingly, flicker filtering which is not beneficial for the graphics image is not performed, and adverse affects to the video image are avoided.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1           1.     A method comprising:  
2                 receiving an alpha value, wherein the alpha value indicates how a  
3 video signal and a graphics signal are to be combined; and  
4                 adjusting a flicker filter based upon the alpha value.

1           2.     The method of claim 1, further comprising:  
2                 comparing the alpha value to a predetermined threshold value to  
3 arrive at a result; and  
4                 adjusting a filter level of the flicker filter in response to the result.

1           3.     The method of claim 2, further comprising:  
2                 subtracting the alpha value from the threshold value to arrive at a  
3 second result.

1           4.     The method of claim 3, further comprising:  
2                 dividing the second result by an alpha step value to arrive at a third  
3 result; and  
4                 adjusting the filter level based on the third result.

1           5.     The method of claim 2, further comprising:  
2                 turning off the flicker filter when the predetermined threshold value  
3 exceeds the alpha value.

1           6.     The method of claim 2, further comprising:  
2                 adjusting the filter level when the alpha value exceeds the  
3     predetermined threshold value.

1           7.     The method of claim 2, further comprising:  
2                 turning off the flicker filter when the graphics image displayed with  
3     the video image is substantially transparent.

1           8.     The method of claim 3, further comprising:  
2                 turning off the flicker filter when the graphics image displayed with  
3     the video image has an alpha value that is below the predetermined threshold  
4     value.

1           9.     The method of claim 1, further comprising:  
2                 evaluating the graphics signal to produce a threshold value;  
3                 comparing the alpha value to the threshold value to arrive at a  
4     result; and  
5                 adjusting a filter level of the flicker filter in response to the result.

1           10.    A system comprising:  
2                 a controller to associate an alpha value with a signal to be  
3     displayed; and  
4                 a processor coupled to the controller for executing a software  
5     program to adjust a flicker filter based upon the alpha value.

1           11. The system of claim 10, wherein the flicker filter operates at a  
2 plurality of levels.

1           12. The system of claim 11, wherein the software program further:  
2 compares the alpha value to a predetermined threshold value to  
3 produce a result; and  
4 adjusts one of the plurality of levels of the flicker filter based upon  
5 the result.

1           13. The system of claim 10, wherein the signal is a mixed video and  
2 graphics signal.

1           14. The system of claim 13, wherein the alpha value specifies how  
2 strongly the graphics signal is to be displayed.

1           15. The system of claim 12, wherein the flicker filter is turned off when  
2 the predetermined threshold value exceeds the alpha value.

1           16. The system of claim 11, wherein the software program further:  
2 evaluates the signal to produce a threshold value;  
3 compares the alpha value to the threshold value to produce a  
4 result; and  
5 adjusts one of the plurality of levels of the flicker filter based upon  
6 the result.

1           17. An article comprising a medium storing instructions that, upon  
2 execution, enable a processor-based system to:  
3           receive an alpha value, wherein the alpha value indicates how a  
4 video signal and a graphics signal are to be combined; and  
5           adjust a flicker filter based upon the alpha value.

1           18. The article of claim 17, further storing instructions that, upon  
2 execution, enable a processor-based system to:  
3           compare the alpha value to a predetermined threshold value to  
4 arrive at a result; and  
5           adjust a filter level of the flicker filter based on the result.

1           19. The article of claim 18, further storing instructions that, upon  
2 execution, enable a processor-based system to subtract the alpha value from the  
3 threshold value to arrive at a second result.

1           20. The article of claim 19, further storing instructions that, upon  
2 execution, enable a processor-based system to:  
3           divide the second result by an alpha step value to arrive at a third  
4 result; and  
5           adjust the filter level based on the third result.



1           21. The article of claim 17, further storing instructions that, upon  
2 execution, enable a processor-based system to:  
3           turn off the flicker filter when the predetermined threshold value  
4 exceeds the alpha value.

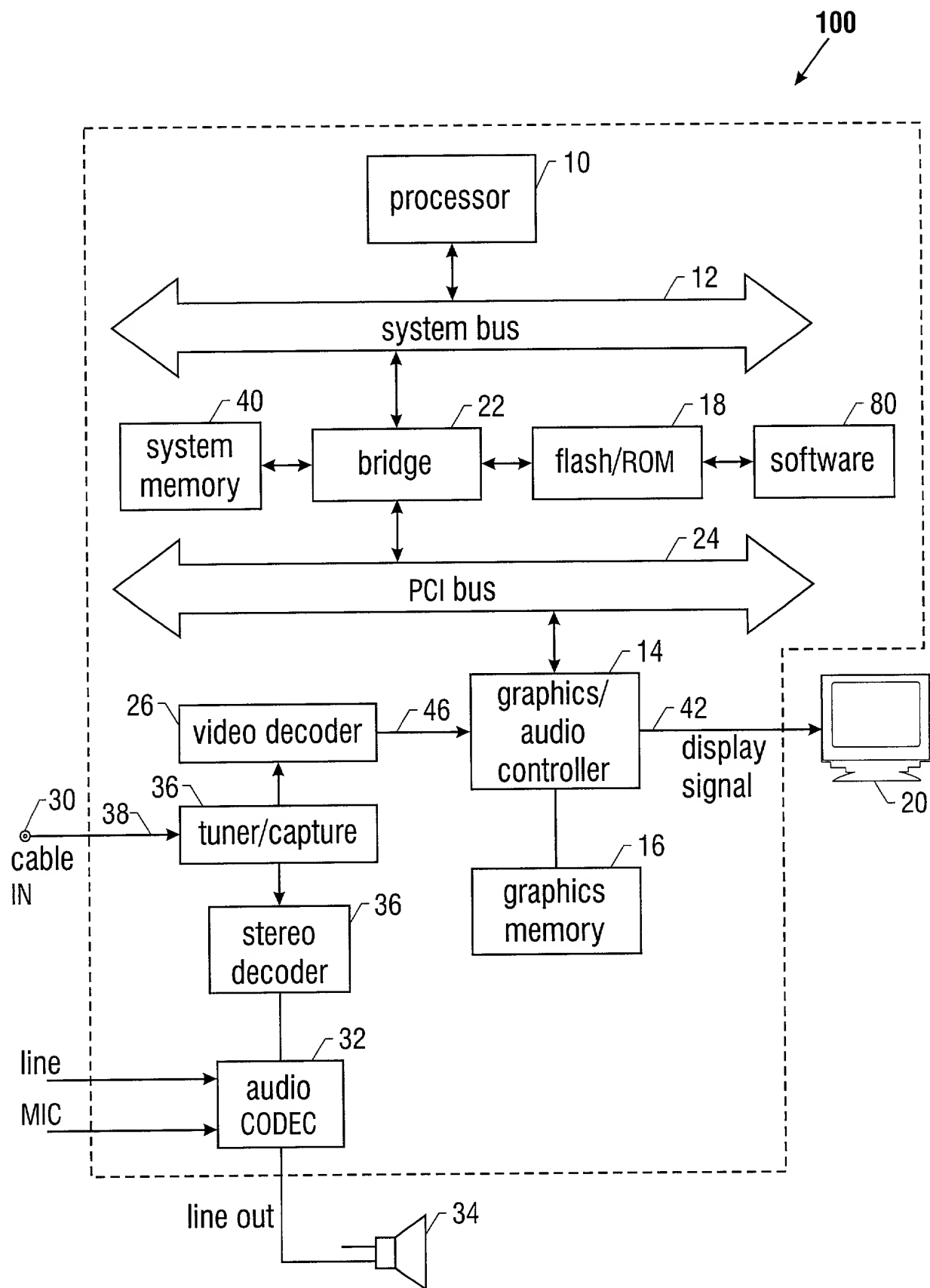
1           22. The article of claim 17, further storing instructions that, upon  
2 execution, enable a processor-based system to:  
3           adjust the filter level when the alpha value exceeds the  
4 predetermined threshold value.

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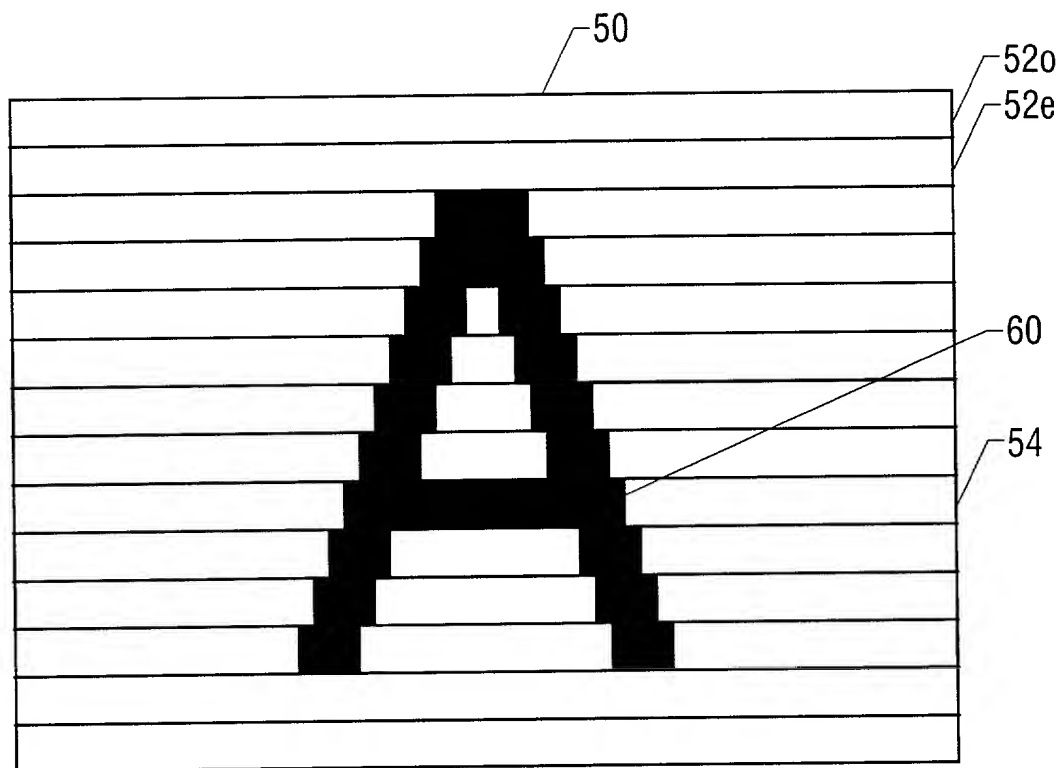
## ANALYZING ALPHA VALUES FOR FLICKER FILTERING

### Abstract of the Disclosure

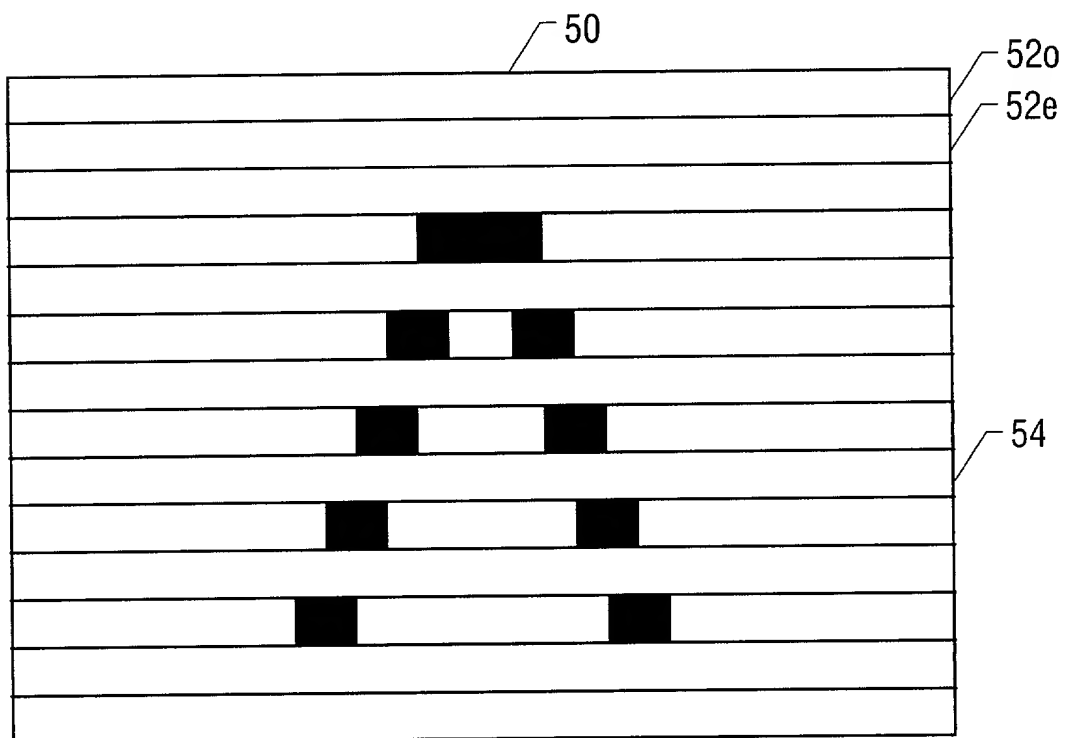
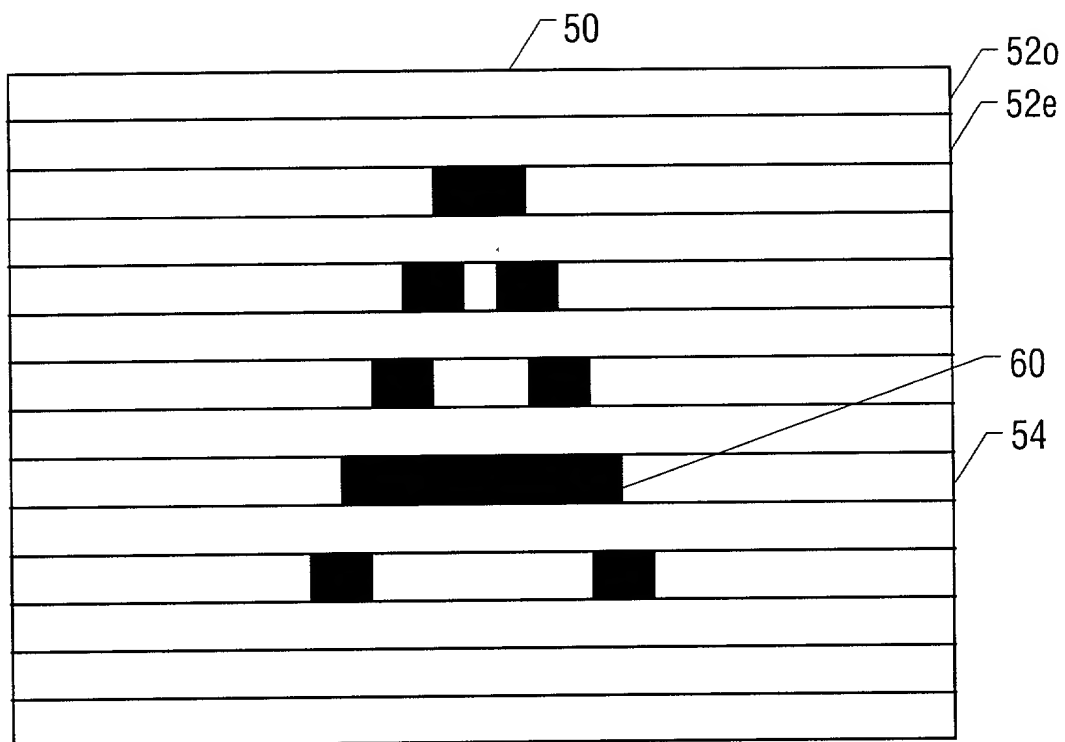
A flicker filter is adjusted according to degree of alpha blending performed on a display signal. For some weakly showing graphics images, a lower flicker filter level may be implemented or the flicker filter may be turned off. A  
5 threshold for turning off the flicker filter may be programmable.

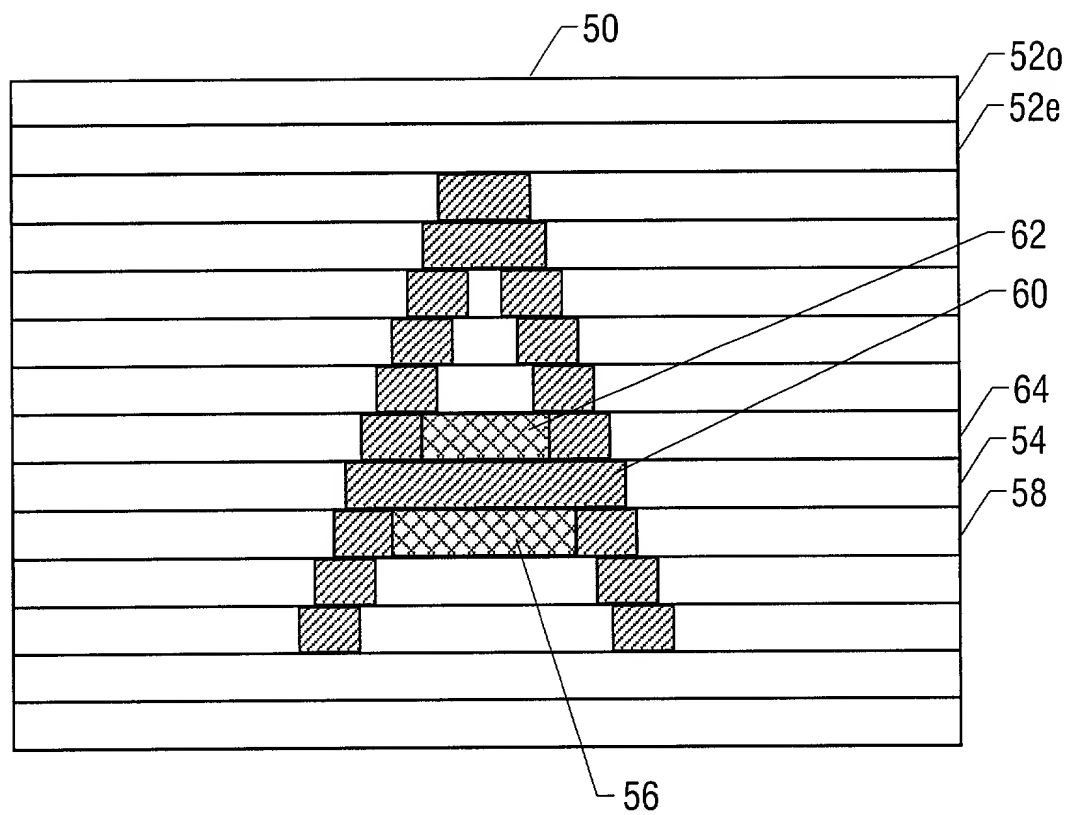


**FIGURE 1**



**FIGURE 2**





**FIGURE 4**

alpha value	flicker filter level
0 - 32	0
33 - 40	1
41 - 48	2
49 - 56	3
57 - 64	4
65 - 72	5
73 - 80	6
81 - 255	7

**FIGURE 5**

alpha value	flicker filter level
0 - 80	0
81 - 88	1
89 - 96	2
97 - 104	3
105 - 112	4
113 - 120	5
121 - 128	6
129 - 255	7

**FIGURE 7**

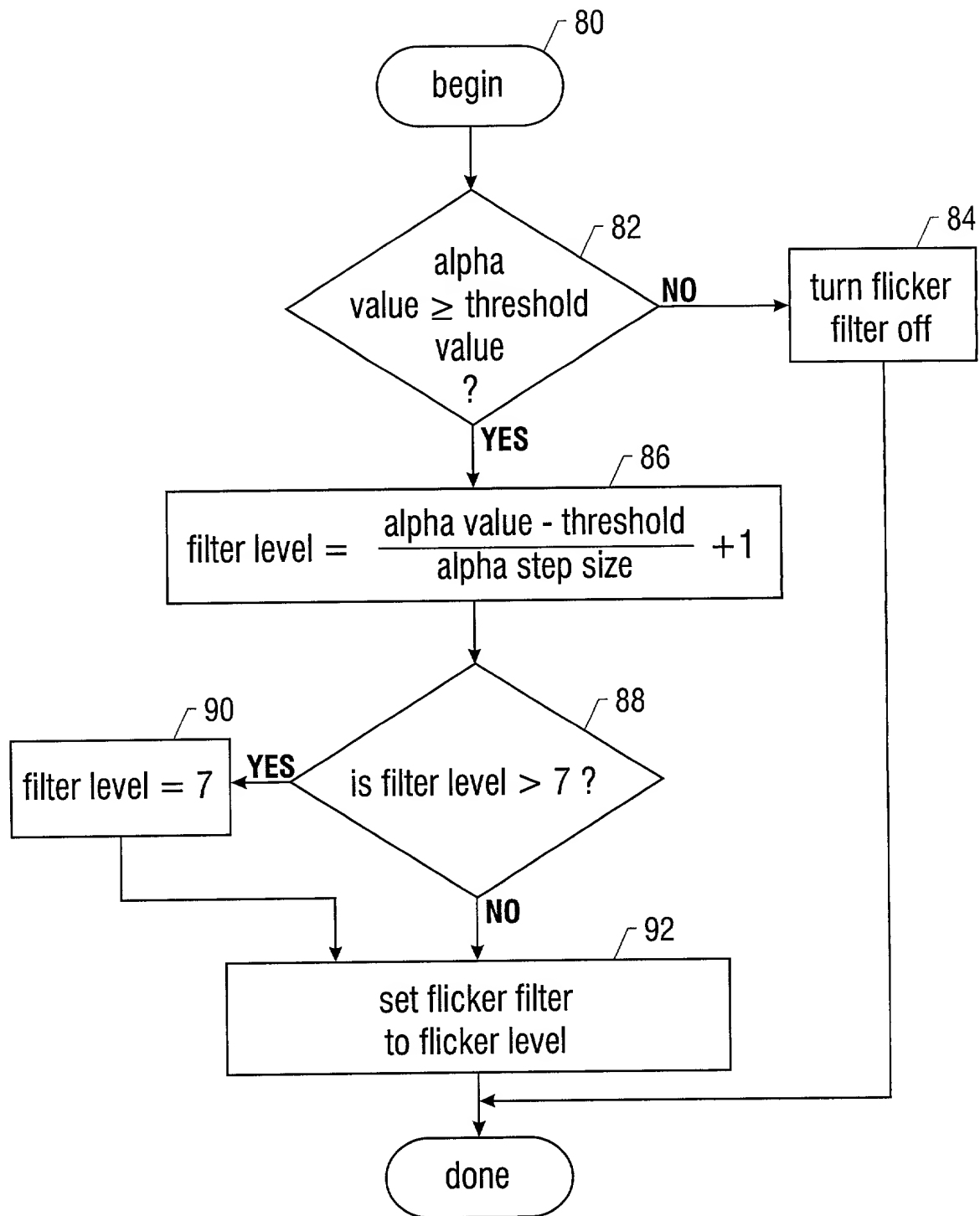


FIGURE 6



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ANALYZING ALPHA VALUES FOR FLICKER FILTERING

the specification of which

X	is attached hereto.
	was filed on _____ as
	United States Application Number _____
	or PCT International Application Number _____
	and was amended on _____
	(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate Issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of the United States provisional application(s) listed below:

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

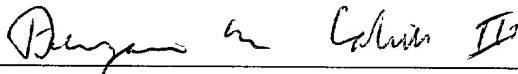
I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

_____ (Application Number)	_____ Filing Date	_____ (Status-patented, pending, abandoned)
_____ (Application Number)	_____ Filing Date	_____ (Status-patented, pending, abandoned)

I hereby appoint Timothy N. Trop, Reg. No. 28,994; Fred G. Pruner, Jr., Reg. No. 40,779 and Dan C. Hu, Reg. No. 40,025 my patent attorneys, of TROP, PRUNER & HU, P.C., with offices located at 8554 Katy Freeway, Ste. 100, Houston, TX 77024, telephone (713) 468-8880, and Mirho, Charles A.; Registration No. 41,199; Novakoski, Leo V.; Registration No. 37,198; Reynolds, Thomas C.; Registration No. 32,488; Seddon, Kenneth M.; Registration No. 43,105; Seeley, Mark; Registration No. 32,299; Skabrat, Steven P.; Registration No. 36,279; Skaist, Howard A.; Registration No. 36,008; Su, Gene I.; Registration No. 45,140; Wells, Calvin E.; Registration No. 43,256; Werner, Raymond J.; Registration No. 34,752; Winkle, Robert G.; Registration No. 37,474; and Young, Charles K.; Registration No. 39,435 my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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INTL-0438-US (P9450)